IN THE CLAIMS:

Please amend claims 1, 2, 5, 6, 9, 10, 12-14 and 17-19 as indicated in the following:

1. (Currently Amended) A method of comprising ~~the steps of~~:

providing a portion of data in response to a counter value being reached, wherein the counter value is stored in a counter that is being incremented at a predetermined rate;

determining a current bit rate;

determining [[an]]a desired bit rate over an amount of time;

determining a running average based on the current bit rate and the desired bit rate, wherein the running average is further based on a difference between a plurality of desired bit rates and current bit rates; and

setting the counter value based on the running average.

2. (Currently Amended) The method of claim 1, wherein ~~the steps of~~ determining and setting are repeated at a predetermined interval rate.

3. (Original) The method of claim 2, wherein the predetermined interval less than approximately 150 milliseconds.

4. (Original) The method of claim 2, wherein the predetermined interval less than approximately 10 milliseconds.

5. (Currently Amended) The method of claim 1, wherein ~~the step of~~ setting the counter value includes using the running average to access a counter value stored in a table.

6. (Currently Amended) The method of claim 1, wherein ~~the step of~~ setting the counter value includes using the running average in an equation to determine the counter value.

7. (Original) The method of claim 1, wherein the data is a portion of a packetized multimedia data stream.

8. (Original) The method of claim 1, wherein the portion of data is a data word having a predetermined width.

9. (Currently Amended) The method of claim 1, wherein the counter value is stored in a register of a first data processor, and ~~step of~~ setting the counter is performed by a host data processor that is different than the first data processor.

10. (Currently Amended) The method of claim 1 further including ~~the step of~~ initializing the counter value to a first count based on a calculated time difference, wherein the calculated time difference is based on clock values stored in the data.

11. (Original) The method of claim 10, wherein the first count is further based upon an amount of data stored between the clock values used to determine the time difference.

12. (Currently Amended) The method of claim 10, wherein ~~the step of~~ providing includes providing the portion of data to an MPEG audio decoder.

13. (Currently Amended) The method of claim 10, wherein ~~the step of~~ providing includes providing the portion of data to the MPEG video decoder.

14. (Currently Amended) A method of comprising ~~the steps of~~:

reading a portion of data in response to a counter value being reached, wherein the counter value is stored in a counter that is [[being]] incremented at a predetermined rate;

determining a current bit rate;

determining [[an]]a desired bit rate over an amount of time;

determining a difference between the current bit rate and the desired bit rate ~~(current bit rate-desired bit rate)~~; [[and]]

increasing the counter value when the difference is greater than a predefined value; and

decreasing the counter value when the difference is negative.

15. (Original) The method of claim 14, wherein the data is a portion of a packetized multimedia data stream.

16. (Original) The method of claim 14, wherein the portion of data is a data word having a predetermined width.

17. (Currently Amended) The method of claim 14, wherein ~~the step of~~ setting the counter is repeated at a rate less than the predetermined amount of time.

18. (Currently Amended) The method of claim 14, wherein ~~the step of~~ setting the counter occurs at a repeated interval.

19. (Currently Amended) A system comprising:

a system bus port to couple to a system bus;

a system clock;

a memory configured as a first in first out memory (FIFO) coupled to [[the]]a data holding register;

a first register coupled to the memory to store a current write location of the [[first]] memory;

a second register coupled to the memory to store a current read location of the [[first]] memory; and

a leak rate controller coupled to the memory to control a rate at which data is read from the memory, the leak rate controller further ~~includes~~ inlcuding

a data rate monitor to determine a current data rate;

a counter coupled to the system clock to provide a read signal when a predefined value is met, wherein the read signal is ~~accesses~~ for accessing data stored in the memory.

20. (Original) The system of claim 19, wherein the leak rate controller further includes a filter coupled to the data rate monitor to determine a running average of a difference between the current data rate and a desired data rate.

21. (Original) The system of claim 19 further comprising an audio decoder coupled to the memory.

22. (Original) The system of claim 20 further comprising a video decoder coupled to the memory.

23. (Original) The system of claim 19 further comprising a video decoder coupled to the memory.